

Appl. No. 10/064,970
Amdt. dated February 06, 2006
Reply to Office action of November 29, 2005

Amendments to the Drawings:

In response to an objection to the drawings, a replacement sheet is submitted, having Figure 6 thereon. The originally submitted Figure 6 was of insufficient quality to distinguish the differences between the dotted line pulses and the solid line pulses. The
5 replacement sheet clearly shows this distinction. No new matter is added through this replacement sheet.

Furthermore, claim 7 has been cancelled, and is no longer in need of consideration
Acceptance of the drawings is respectfully requested.

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Attachment: Replacement Sheet

1 page

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REMARKS/ARGUMENTS

1. Objection to the specification:

The disclosure is objected to due to informalities. Appropriate correction is required.

5 **Response:**

Paragraphs 0005, 0008, 0009, 0023, 0026, 0028, and 0030 of the specification have been amended to correct these informalities. Acceptance of the specification is respectfully requested.

10 2. Objection to the claims:

The claims are objected to due to informalities. Appropriate correction is required.

Response:

15 The claims have been amended to correct the cited informalities. Acceptance of the corrected claims is requested.

3. Rejection of claims 1-5 under 35 U.S.C. 103(a):

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art of the instant application in view of Burdick et al. (US 6,661,271).

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Response:

Claim 1 has been amended to overcome this rejection. Claim 1 now contains limitations previously contained in claims 2 and 3, and no new matter has been added through this amendment.

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Claim 1 now recites that when a status of the serial transmission line remains in a transmit mode, the first and second delay control cells generate a first delay time, and

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when a status of the serial transmission line switches from an idle mode to the transmit mode, the first and second delay control cells generate a second delay time. In addition, claim 1 states that, the first and second delay times are unequal.

- 5 The claimed first and second delay control cells are not merely simple delay cells that always delay a signal by a predetermined amount. Instead, the delay is conditional on the mode of the serial transmission line. Instead of a single delay being produced by the delay cells, two unequal delays are created.
- 10 On the other hand, Burdick teaches in Fig.1 that two flip flops are used as delay cells. Burdick also teaches that the flip flops are used to synchronize the timing between +V and -V. However, each of the flip flops creates a delay that is equal for all signals passing through the flip flop, and does not create two unequal delays depending on the mode of the serial transmission line. Furthermore, Burdick's ability to synchronize the timing
- 15 between +V and -V does not solve the problem that the present invention is addressing, in which different delays are created depending on the mode of the serial transmission line. Since Burdick does not teach delay circuits that create two unequal delay times depending on the mode of the serial transmission line, claim 1 is patentably distinct from the combination of the prior art of the instant application and Burdick.
- 20 Claims 2-5 are dependent on claim 1, and should be allowed if claim 1 is allowed. Reconsideration of claims 1-5 is respectfully requested.

4. Rejection of claims 6-9 under 35 U.S.C. 103(a):

- 25 Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art of the instant application in view of Burdick et al. and further in view of Paschal et al.

Response:

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Claims 6, 8, and 9 are dependent on claim 1, and should be allowed if claim 1 is allowed. Reconsideration of claims 6, 8, and 9 is respectfully requested.

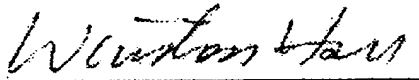
5. Introduction to new claim 10:

- 5 New claim 10 is drafted to claim the structure of the first and second delay control cells. As illustrated in Figure 5 of the instant application, each of the first and second delay control cells comprises a control transistor in parallel with a resistor. The first and second delay times are produced by controlling the control transistor, and thereby changing the path between ends of the delay control cell. The cited prior art does not
- 10 teach that the delay control cells have the structure of a control transistor in parallel with a resistor. Acceptance of claim 10 is respectfully requested.

In view of the above statements in favor of patentability, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,



Date: 02/06/2006

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- 25 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)